REMARKS

Examiner objected to the drawing. In particular, the Examiner stated:

> The drawings are objected to because of draftsperson's remarks (see attached PTO-948 paper 13). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Applicant respectfully submits that the draftsperson's remarks merely relate to formalities which can be corrected after the case is allowed.

In light of the above, Applicant respectfully requests that the Examiner withhold this objection until the case is allowed.

Examiner rejected claims 1-7 under 35 U.S.C. 102(e). In particular, the Examiner stated:

> Claims 1-7, are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al., (US. 5,808,735).
>
> As to claim 1, Lee teaches an image processing system, a method for relating a first image (note, first image is test image) to a second image (note, second image is reference second image) comprising (abstract):
>
> (a) aligning the first image (note, first image is test image) with a second image (note, second image is reference image second image, fig 2A item 210);
>
> (b) plotting a gray level of a pixel from the first image against a gray level of a corresponding pixel from the second image for all aligned pixel locations (note, the test image and the reference images are aligned based on the intensities of the two images. These two images are being compared pixel-by-pixel, the difference in intensities between test and the reference pixels are then used to create an intensity histogram, (column 5, lines 54-66, column 6, lines 21-33).
>
> As per claim 2, Lee teaches the method of claim 1 further comprising plotting (note, the peak value of the intensity histogram represents the most common intensity difference between test and reference pixel, column 11, lines 16-24) a threshold window on a plot created in step (b)(column 6, lines 1-5, column 10, lines 43-57).
>
> As per claim 3, Lee teaches the method of claim 1 wherein a plot created in step (b) is stored in a memory array variable (column 6, lines 41-56).
>
> As per claim 4, Lee teaches the method of claim 1, wherein a plot created in step(b) is displayed on a video monitor (fig. 1, item 60, column 4, lines 20-29).
>
> As per claim 5, Lee teaches a computer-readable medium storing a program for carrying out the method of claim 1 (column 7, lines 5-9).
>
> As per claim 6, Lee teaches a computer-readable medium comprising:

a plurality of memory locations storing (column 7, lines 35-64) data representing a first image and an associated second image (column 7, lines 35-64), said first and second images each having a plurality of pixels with each pixel being defined by a location coordinate (column 7, lines 35-, 31) and a gray level (column 13, lines 4-10); and,

As per claim 7, Lee teaches a defect inspection system comprising:

(a) an image acquisition unit (fig. 1, item 50) being operable to acquire a first image and an associated second image (column 4, lines 45-50) the first and second images each having a plurality of pixels with each pixel being defined by a location coordinate (column 13, lines 4-31) and a gray level (column 2, lines 10-14, column 6, lines 21-33, column 13, lines 4-31);

(b) a plurality of memory locations storing data representing the first image and the second image (column 6, lines 41-56); and

(c) a processor (fig. 1, item 20) being operable to plot the gray levels of pixels from the first image against the gray levels of corresponding pixels from the second image (note, the test image and the reference images are aligned based on the intensities of the two images. These two images are being compared pixel-by-pixel, the difference in intensities between test and the reference pixels are then used to create an intensity histogram (column 5, lines 54-66, column 6, lines 21-33).

Applicants respectfully traverses the Examiner's rejection.

Regarding claim 1: Applicant respectfully submits that Lee et al. teaches method and apparatus that is completely different from claim 1 which requires plotting a gray level of a pixel from the first image **against** a gray level of a corresponding pixel from the second image for all aligned pixel locations.

In particular, as set forth at col. 5, lines 54-67, Lee et al. teaches that defects are detected by aligning test and reference images and then subtracting the images one from the other. Intensity differences between corresponding test and reference pixels that exceed an intensity-error threshold indicate the presence of a defect. Specifically, as set forth at col. 6, lines 21-30, Lee et al. discloses:

> The test and reference images are aligned and their relative intensities are compared pixel-by-pixel. The x-y locations of any test and reference pixel pair P_T, P_R having intensity values I_{MAX} that differ by an amount exceeding the intensity-error threshold I_{TH} assigned to the x-y locations are identified as potential defect pixels. The **intensity differences** of the remaining pixels are then used to create an intensity histogram. The peak value of the intensity histogram represents the most common intensity

difference between test and reference pixel pairs P_T, P_R. (Emphasis added)

Specifically, as set forth at col. 6, lines 41-56, Lee et al. discloses:

> Once the test and reference images are aligned in three dimensions and normalized for intensity, the intensity values I_{max} of corresponding test and reference images are compared pixel-by-pixel (step 235) pixels using the intensity-error threshold I_{TH} assigned to the z level associated with the reference pixel. The x-y locations of corresponding pixels having intensity values $P_T(I_{max})$ and $P_R(I_{max})$ that differ by an amount exceeding the intensity-error threshold I_{TH} are stored in memory as an array of potential defect pixels (the defect array D). In one embodiment, the defect array D is represented in memory using a single binary bit for each pixel: a logic one or a logic zero respectively represents the presence or absence of a defect at a given x-y location. Alternatively, a defect array may be represented in memory using multiple bits to store the intensity and/or Z difference associated with each defect pixel.

As the Examiner can readily appreciate from this, Lee et al. provides no teaching, disclosure or suggestion of any kind for plotting a gray level of a pixel from the first image **against** a gray level of a corresponding pixel from the second image for all aligned pixel locations as required by claim 1. Applicant respectfully submits that Lee et al. does not disclose, teach, hint or suggest, in any manner whatsoever, making the unique plot required by claim 1 because the difference identification taught by Lee et al. is completely different from the unique plot created in accordance with claim 1. As such, Applicant respectfully submits that Lee et al. does not anticipate claim 1.

Regarding claim 2: Applicant respectfully submits that claim 2 depends from claim 1, and that claim 2 is patentable over Lee et al. for the reasons set forth above with respect to claim 1. In addition, Applicant respectfully submits that Lee et al. does not teach plotting a threshold window on a plot of gray levels of pixels from the first image **against** gray levels of corresponding pixels from the second image for all aligned pixel locations as required by claim 2. In particular, Applicant respectfully submits that Lee does not teach plotting a threshold. Applicant respectfully submits that col. 10, line 29 to col. 11, line 2 of Lee et al. discloses a

process of establishing multiple error thresholds I_{TH} but does not teach, disclose or suggest in any manner plotting a threshold as required by claim 2. As such, Applicant respectfully submits that Lee et al. does not anticipate claim 2.

Regarding claim 3: Applicant respectfully submits that claim 3 depends from claim 1, and that claim 3 is patentable over Lee et al. for the reasons set forth above with respect to claim 1. In addition, Applicant respectfully submits that Lee et al. does not teach storing a plot as required by claim 3. In particular, as was set forth above, Lee et al. merely teaches storing a defect array at col. 6, lines 46-56 as follows: "The x-y locations of corresponding pixels having intensity values $P_T(I_{max})$ and $P_R(I_{max})$ that differ by an amount exceeding the intensity-error threshold I_{TH} are stored in memory as an array of potential defect pixels (the defect array D). In one embodiment, the defect array D is represented in memory using a single binary bit for each pixel: a logic one or a logic zero respectively represents the presence or absence of a defect at a given x-y location. Alternatively, a defect array may be represented in memory using multiple bits to store the intensity and/or Z difference associated with each defect pixel." As such, Applicant respectfully submits that Lee et al. does not anticipate claim 3.

Regarding claim 4: Applicant respectfully submits that claim 4 depends from claim 1, and that claim 4 is patentable over Lee et al. for the reasons set forth above with respect to claim 1. In addition, Lee et al. does not teach displaying a plot as required by claim 4. In particular, Applicant respectfully submits that FIG. 1 of Lee et al. merely shows a work station without any teaching of displaying a plot as required by claim 4. As such, Applicant respectfully submits that Lee et al. does not anticipate claim 4.

Regarding claim 5: Applicant respectfully submits that claim 5 is patentable over Lee et al. for the reasons set forth above with respect to claim 1. As such, Applicant respectfully submits that Lee et al. does not anticipate claim 5.

Regarding claim 6: Independent claim 6 requires a computer-readable medium that comprises an array of memory locations storing data representing a plot of the gray levels of pixels from the first image **against** the gray levels of corresponding pixels from the second image. As set forth above in regard to claim 1, Applicant respectfully submits that Lee et al. does not teach or hint providing or storing such an array. Specifically, as set forth above,

Applicant respectfully submits that Lee et al. at col. 6, lines 46-56 merely teaches storing a defect array as follows: "The x-y locations of corresponding pixels having intensity values $P_T(I_{max})$ and $P_R(I_{max})$ that differ by an amount exceeding the intensity-error threshold I_{TH} are stored in memory as **an array of potential defect pixels** (the defect array D). In one embodiment, the defect array D is represented in memory using a single binary bit for each pixel: a logic one or a logic zero respectively represents the presence or absence of a defect at a given x-y location. Alternatively, a defect array may be represented in memory using multiple bits to store the intensity and/or Z difference associated with each defect pixel. (Emphasis added)" As such, Applicant respectfully submits that Lee et al. does not anticipate claim 6.

Regarding claim 7: Independent claim 7 requires a processor being operable to plot the gray levels of pixels from the first image **against** the gray levels of corresponding pixels from the second image. As set forth above in regard to claim 1, Applicant respectfully submits that Lee et al. does not teach or hint providing such a processor. As such, Applicant respectfully submits that Lee et al. does not anticipate claim 7.

In light of the above, Applicant respectfully requests that the Examiner withdraw this rejection.

In light of the above, Applicants respectfully submit that all the remaining claims are allowable, and Applicants respectfully request that the Examiner reconsider the case and pass the case to issue. Should the Examiner have any questions or wish to discuss any aspect of the application, a telephone call to the undersigned would be welcome.

Respectfully submitted,

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